



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,184	04/02/2004	David L. Linam	AG10031083-1	2153
22878	7590	05/12/2005	EXAMINER	
AGILENT TECHNOLOGIES, INC. INTELLECTUAL PROPERTY ADMINISTRATION, LEGAL DEPT. P.O. BOX 7599 M/S DL429 LOVELAND, CO 80537-0599			LAM, TUAN THIEU	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

27

Office Action Summary	Application No. 10/817,184	Applicant(s) LINAM ET AL.	
	Examiner Tuan T. Lam	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 April 2004 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 4, the recitation of "the storage node" in line 2 lacks proper antecedent basis.

In claim 6, the recitation of "the storage node" in lines 3-4 lacks proper antecedent basis.

In claim 7, the recitation of "the storage node" in line 2 lacks proper antecedent basis.

Claims 5 are indefinite because of the technical deficiencies of claim 4.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 7-8 and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by (JP 5-37305). Figure 1 shows differential register comprising an output node and complementary output node (NQ, Q), a storage node (G) coupled between the output node and the complimentary output node, the method comprising the step of storing a first value in the storage node, storing the compliment of the first value in the storage node and on power up, conveying the first value stored in the storage node out of the output node and conveying the

Art Unit: 2816

compliment of the first value stored in the storage node (H) out of the complement of the output node as called for in claim 15.

Regarding claim 16, the circuit of JP 5-37305 is capable of performing the recited functions.

Regarding claims 1 and 17, figure 1 shows an input means (D) for conveying an input signal, a first pass means (101), a first signal (G), a second pass means (102), storage means (107), first output means (105), a second output means (106).

Regarding claim 2, the first and second devices are controlled by the same clock signal.

Regarding claims 7-8, the first and second inverters are seen as inverters 105 and 106 of figure 1.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4, 6-8 and 15-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Chalasani (USP 6,864,732). Figure 2A shows differential register comprising an output node and complementary output node (DATAB_OUT and DATA_OUT), a storage node (cross coupled inverters of the second stage 151) coupled between the output node and the complementary output node, the method comprising the step of storing a first value in the storage node, storing the compliment of the first value in the storage node and on power up, conveying the first value stored in the storage node out of the output node and conveying the compliment of the first value stored in the storage node (H) out of the complement of the output node as called for in claim 15.

Regarding claim 16, the circuit of figure 2A is capable of performing the recited

Art Unit: 2816

functions.

Regarding claims 1, 17, figure 1 shows an input means (input to transistor 115) for conveying an input signal, a first pass means (115), a first signal (output of the transistor 115), a second pass means (117), storage means (two cross coupled inverter of the second stage 151), first output means (inverter coupled to provide DATAB_OUT), a second output means (inverter coupled to provide DATA_OUT).

Regarding claim 2, the first and second devices are controlled by the same clock signal.

Regarding claims 7-8, the first and second inverters are seen as inverters providing DATAB_OUT and DATA_OUT in figure 2A.

Regarding claim 3, a second storage node (two cross coupled inverters of the first stage 201).

Regarding claim 4, an input pass device (211).

Regarding claim 6, figure 2A shows a first inverter (inverter connected to the bottom transistor of the passing transistors 115).

6. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by Mokovic et al.(US 2003/0107421).

Figure 1 shows an input signal (80), a first pass gate (20), a master clock signal (CN), a first storage node (output of the transistor 20), a second pass gate (30), a slave clock (CP), a first inverter (120), a third pass gate (bottom transistor of passing gate 30), a second storage node (output of the transistor 30) as called for in claim 9.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chalasani (USP 6,864,732) in view of Shikata et al. (USP 4,939,384).

Figure 2A of Chalasani shows a differential register comprising all the limitations recited in claim 1 except Chalasani's register is controlled by a single clock signal (CLK) instead of a differential clock signals as called for in claim 5. It is noted that Chalasani uses a single clock signal to control a complementary passing transistors (111 and 115) in a differential register (master and slave latch). This is functionally equivalent to having a same type of passing transistors being controlled by complementary clock signals. This equivalent functionality is well demonstrated in Shikata et al. (USP 4,939,384). Figure 1 of Shikata et al. use channel type passing transistors (1, 2, 7 and 8). The n channel type passing transistors are controlled by a complementary clock signals (CL and CL/). The N channel transistors are, in part, faster than the P channel transistor due to the fact that N channel transistors have more electrons than the p channel transistors. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to replace the P channel passing transistors (111) of Chalasani with N channel passing transistors and being controlled by a complementary clock as taught by Shikata et al. for the purpose of increasing speed.

Art Unit: 2816

9. Claims 10-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mokovic et al.(US 2003/0107421).

Figure 1 of Mokovic et al. shows all the limitations of claim 9 as noted above except for a third inverter coupled to the second storage node, the third inverter generating a complement output signal as called for in claim 10. As noted in figure 1 of Mokovic et al., the master and slave latch provides a single output signal by an inverter connected to an input of the inverter 50. Such a single output master and slave latch can be easily converted to a differential master and slave latch. One of common way of doing so is to couple an extra inverter at the output of the inverter 50 of Mokovic et al. Depending on application, a differential output signals can be provided. Therefore, outside of an non-obvious results, the obviousness of using an extra inverter to provide a complement output signal in a master and slave latch will not be patentable under 35USC 103(a).

Regarding claim 11, figure 1 of Mokovic et al. shows a fourth and fifth inverters (upper and lower inverters of the latch 40, respectively).

Regarding claim 12, figure 1 of Mokovic et al. shows sixth and seventh inverters (upper and lower inverters of the latch 50, respectively) but does not disclose the sixth inverter is weaker than the fourth inverter. However, it is known to have the upper inverter of the master stage bigger than the upper inverter of the slave stage in order to overcome the signal of the subsequent stage (slave stage) in order to prevent erroneous operation. Therefore, outside of an non-obvious results, the obviousness of having inverter of different size will not be patentable under 35USC 103(a).

Regarding claim 13, figure 1 of Mokovic et al. shows fourth and fifth inverters (upper and lower inverter of the latch 50).

Regarding claim 14, figure 1 of Mokovic et al. shows fourth and fifth inverters (upper and lower inverter of the latch 50).but does not disclose the fourth inverter is weaker than the first inverter (120). However, it is known to have the input inverter (120) bigger than the inverter of a latch within the master and slave register in order to overcome the signal within the latch in order to prevent erroneous operation. Therefore, outside of an non-obvious results, the obviousness of having inverter of different size will not be patentable under 35USC 103(a).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2816

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Tuan T. Lam', with a long horizontal flourish extending to the right.

Tuan T. Lam
Primary Examiner
Art Unit 2816

5/11/2005